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BONDPAD ATTACHMENTS ~~USED TO TEMPORARILY CONNECT~~ SEMI~~CO~~NDUCTOR DIE

~~CROSS-REFERENCE TO RELATED APPLICATION~~

Ins. A2

~~This is a continuation-in-part to U.S. Patent Application No. 7/709,858, filed 6/4/91, U.S. Patent Application No. 7/788,065, filed 11/05/91, and U.S. Patent Application No. 7/981,956, filed 11/24/92.~~

Ins. A3

BACKGROUND OF THE INVENTION

Ins. A4

Field of the Invention

This invention relates to electrical test equipment for semiconductor devices. More specifically, the invention relates to an apparatus and method, which utilize conductive polymers, and which are used to perform dynamic burn-in and full electrical/performance/speed testing on discrete nonpackaged or semi-packaged dies.

Background of the Invention

Semiconductor devices are subjected to a series of test procedures in order to assure quality and reliability. This testing procedure conventionally includes "probe testing", in which individual dies, while still on a wafer, are initially tested to determine functionality and speed. Probe cards are used to electrically test die at that level. The electrical connection interfaces with only a single die at a time in wafer; not discrete die.

If the wafer has a yield of functional dies which indicates that quality of the functional dies is likely to be good, each individual die is assembled in a package to form a semiconductor device. Conventionally, the packaging includes a lead frame and a plastic or ceramic housing.

The packaged devices are then subjected to another series of tests, which include burn-in and discrete testing. Discrete testing permits the devices to be tested for speed and for errors which may occur after assembly and after burn-in. Burn-in accelerates failure mechanisms by electrically exercising the devices (DUT) at elevated temperatures, thus eliminating potential failures which would not otherwise be apparent at nominal test conditions.

Variations on these procedures permit devices assembled onto circuit arrangements, such as memory boards, to be burned-in, along with the memory board in order to assure reliability of the circuit, as populated with devices. This closed assembly testing assumes that the devices are discretely packaged in order that it can then be performed more readily.

If the wafer has a yield of grossly functional die, it indicates that a good quantity of die from the wafer are likely to be fully operative. The die are separated with a die saw, and the nonfunctional die are scrapped, while the rest are individually encapsulated in plastic packages or mounted in ceramic packages with one die in each package. After the die are packaged they are rigorously electrically

tested. Components which turn out to be nonfunctional, or which operate at questionable specifications, are scrapped or devoted to special uses.

Packaging unusable die, only to scrap them after testing, is a waste of time and materials, and is therefore costly. Given the relatively low profit margins of commodity semiconductor components such as dynamic random access memories (DRAMs) and static random access memories (SRAMs), this practice is uneconomical. However, no thorough and cost effective method of testing an unpackaged die is available which would prevent this unnecessary packaging of nonfunctional and marginally functional die. Secondly, the packaging may have other limitations which are aggravated by burn-in stress conditions, so that the packaging becomes a limitation for burn-in testing.

It is proposed that multiple integrated circuit devices be packaged as a single unit, known as a multi chip module (MCM). This can be accomplished with or without conventional lead frames. This creates two problems when using conventional test methods. Firstly, discrete testing is more difficult because a conventional lead frame package is not used. Furthermore, when multiple devices are assembled into a single package, the performance of the package is reduced to that of the die with the lowest performance. Therefore, such dies are tested on an individual basis at probe, using ambient and "hot chuck" test techniques, while still in wafer form. In other words, the ability to presort the individual dice is limited to that obtained through probe testing.

In addition, there is an increased interest in providing parts which are fully characterized prior to packaging. This is desired not only because of the cost of the package, but also because there is demand for multi-chip modules (MCMs), in which multiple parts in die form are tested and assembled into a single unit. While there are various techniques proposed for testing, burning in and characterizing a singulated die, it would be advantageous to be able to "wafer map" the die prior to assembly with as many performance characteristics as possible. Ideally, one would want to be able to map the wafer with full device characterization.

MCMs create a particular need for testing prior to assembly, as contrasted to the economics of testing parts which are discretely packaged as singulated parts. For discretely packaged parts, if the product yield of good parts from preliminary testing to final shipment (probe-to-ship) is, for example, 95%, one would not be particularly concerned with packaging costs for the failed parts, if packaging costs are 10% of the product manufacturing costs. Even where packaging costs are considerably higher, as in ceramic encapsulated parts, testing unpackaged die is economical for discretely packaged parts when the added costs approximates that of cost of packaging divided by yield:

$$C_{DIE} \times \frac{C_{PACKAGE}}{\text{Yield}} = C_{DIE} \times C_{ADDL.\ KGD}$$

where C = cost
C_{DIE} = manufacturing cost of functional die
$C_{ADDL.\ KGD}$ = additional cost of testing unpackaged die in order to produce known good die (KGD)

Note that in the case of discretely packaged parts, the cost of the die (C_{DIE}) is essentially not a factor. This changes in the case of MCMs:

$$(C_{DIE}) \times \frac{\text{(number of die)}}{\text{Yield}} \times C_{PACKAGE} = C_{DIE} \times C_{ADDL.\ KGD}$$

Note that again C_{DIE} is not a factor in modules having identical part types; however, the equation must be modified to account for varied costs and yields of die in modules with mixed part types.

With MCMs, the cost of packaging a failed part is proportional to the number of die in the module. In the case of a x16 memory array module, where probe-to-ship yield of the die is 95%, the costs are:

$$\frac{16}{0.95} \times C_{PACKAGE} = C_{ADDL.\ KGD}$$

so the additional costs of testing for known good die (KGD) may be 16 times the cost of testing an unrepairable module and still be economical. This, of course, is modified by the ability to repair failed modules.

Testing of unpackaged die before packaging into multichip modules would be desirable as it would result in reduced material waste, increased profits, and increased throughput. Using only known good die in MCMs would increase MCM yields significantly.

Testing unpackaged die requires a significant amount of handling. Since the test package must be separated from the die, the temporary packaging may be more complicated than either standard discrete packaging or multichip module (MCM) packaging. The package must be compatible with test and burn-in procedures, while securing the die without damaging the die at the bondpads or elsewhere during the process.

In U.S. Patent 4,899,107, commonly assigned, a reusable burn-in/test fixture for discrete TAB die is taught. The fixture consists of two halves, one of which is a die cavity plate for receiving semiconductor dies as the units under test (UUT); and the other half establishes electrical contact with the dies and with a burn-in oven.

The first half of the test fixture contains cavities in which die are inserted circuit side up. The die will rest on a floating platform. The second half has a rigid high temperature rated substrate, on which are mounted probes for each corresponding die pad. Each of a plurality of probes is connected to an electrical trace on the substrate (similar to a P.C. board) so that each die pad of each die is electrically isolated from one another for high speed functional testing purposes. The probe tips are arranged in an array to accommodate eight or sixteen dies.

The two halves of the test fixture are joined so that each pad on each die aligns with a corresponding probe tip. The test fixture is configured to house groups of 8 or 16 die for maximum efficiency of the functional testers.

There are some testing and related procedures when the parts are singulated. For this reason, it is inconvenient to retain multiple die in a single test fixture.

Various forms of connections are used to connect the die to a package or, in the case of a multichip module (MCM), to other connections. These include wirebonding, TAB connections, bump bonding directly to substrate, and conductive adhesives.

The bondpads are conductive areas on the face of the die which are used as an interconnect for connecting the circuitry on the die to the outside world. Normally, conductors are bonded to the bondpads, but it is possible to establish electrical contact through the bondpads by biasing conductors against the bondpads without actual bonding.

One of the problems encountered with burn in and full characterization testing of unpackaged die is the physical stress caused by connection of the bondpads to an external connection circuitry. This problem is complicated by the fact that in many die configurations, the bondpads are recessed below the surface level of a passivation layer. The passivation layer is a layer of low eutectic glass, such as BPSG, which is applied to the die in order to protect circuitry on the die. (The term "eutectic" does not, strictly speaking, apply to glass, which is an amorphous fluid; however, the term is used to describe the characteristic of some glasses wherein, as a result of their formulation, they readily flow at a given temperature.)

The ohmic contact between bondpads or test points on a die and a known good die test carrier package has been a matter of interest. It is difficult to achieve and maintain consistent ohmic contact without damaging the bondpads and passivation layer on the die. The design criteria of such contacts is somewhat different from the design criteria of the carrier package.

Summary of the Invention

It has been found desirable to perform testing and related procedures in discrete fixtures prior to final assembly. In order to accomplish this, a reusable burn-in/test fixture for discrete die is provided. The fixture preferably consists of two halves, one of which is a die cavity plate for receiving a semiconductor die as the units under test (UUT).

An intermediate substrate is used to establish ohmic contact with the die at bondpads or testpoints. The intermediate substrate is connected to conductors on the reusable test fixture, so that the bondpads or testpoints are in electrical communication with the conductors on the test fixture.

The intermediate substrate is preferably formed of a semiconductor material, and includes circuitry which is used to conduct signals between bondpad locations and external connector leads on the fixture. The substrate with circuitry is able to establish contact with the external connector

leads, or with other leads on the fixture which are in communication with the external connector leads. In the preferred embodiment, the substrate is formed from silicon, although other semiconductor materials may be used. Examples of alternative materials include germanium and silicon on saphire (SOS).

The substrate is formed with portions having increased height, such as bumps. These bumps, in turn, are formed with raised portions or points, so that the raised portion may penetrate the bondpad by at least 5000Å, while the remainder of the bump functions to limit penetration depth of the raised portion. This permits the penetration depth of the bump to be controlled by the physical dimensions of the raised portion. This results in the bumps being self-limiting in their penetration of the bondpads.

In a modification of the invention, a Z-axis anisotropic conductive interconnect material is provided as an interface between the substrate and the die. The Z-axis anisotropic conductive interconnect material is used to establish ohmic contact with bondpads or the equivalent attach points on the semiconductor die. The Z-axis anisotropic conductive interconnect material is able to conform to the shape of the die at the bondpad sufficiently to establish the ohmic contact without substantially damaging the bondpad. Since contact is able to be established by biasing force, it is possible to perform burn in and test of the die without resorting to bonding a conductor to the bondpad.

The Z-axis anisotropic conductive interconnect material is a metal filled polymer composite which is able to function as a compliant interconnection material for connector and testing applications. This material is in a group of materials which are referred to as elastomeric conductive polymer interconnect (ECPI) materials. These are available from AT&T Bell Laboratories, of Allentown, Pennsylvania, or Shin Etsu Polymer America Inc., of Union City, California, 3M Company of Minneapolis, Minnesota, at their Austin, Texas plant or Nitto Denko America, Inc., San Jose, California (a subsidiary of Nitto Denko Corporation of Japan).

The contact between the bondpads and the external connector leads is therefore established by utilizing the Z-axis anisotropic conductive interconnect material and substrate with circuitry. Conductors on the Z-axis anisotropic conductive interconnect material and substrate with circuitry extend from the bondpads to connection points, and the connection points conduct to contacts, which are in turn in communication with the external connector leads. The self-limiting nature of the bump is transferred through the Z-axis anisotropic conductive interconnect material so that the potential damage to the bondpad by force exerted through the Z-axis anisotropic conductive interconnect material is limited.

In a preferred embodiment, the intermediate substrate is placed in the die receiving cavity and is electrically connected to conductors on the fixture, which in turn are connected to the connector pins. The die is placed face down in the die receiving cavity. The substrate is attached to

conductors on the fixture, which in turn are connected to the connector pins. Ohmic contact is established between bondpads or testpoints on the die and conductors on the substrate.

Z-axis anisotropic conductive interconnect material may be placed in the die receiving cavity beneath the die so that the ohmic contact with the bondpads or testpoints on the die may be established through the Z-axis anisotropic conductive interconnect material, through the substrate, to communicate with external connector leads on the fixture.

In an alternate embodiment, a die is placed face up in a cavity in a first half of the fixture, and the semiconductor substrate is placed over the die. In the preferred form of that embodiment, the external connector leads are connector pins, which preferably are in a DIP (dual inline package) or QFP (quad flat pack) configuration. The pins terminate at the connection points.

The fixture establishes electrical contact with the a single die and with a burn-in oven, as well as permitting testing of dies in discretely packaged form.

If the die is placed face up in a cavity in a first half of the fixture, the substrate may be placed between the die and a lid. Attachment of the die to the external connection leads is established either through contact points on the substrate, or through the contact points through the Z-axis anisotropic conductive interconnect material, in which case, the substrate establishes contact with the Z-axis anisotropic conductive interconnect material.

Brief Description of the Drawings

Figures 1 and 2 show a preferred embodiment of the inventive burn-in fixture;

Figure 3 shows details of an intermediate substrate formed of silicon according to the invention;

Figure 4 shows details of electrical ohmic contact of the substrate with bondpads on a die;

Figure 5 shows details of an intermediate substrate formed from a ceramic material with conductive traces;

Figure 6 shows details of a raised portion of a bump, wherein the bump may be self-limiting in its penetration of the bondpads;

Figure 7 shows details of Z-axis anisotropic conductive interconnect material and an intermediate substrate used with one embodiment of the invention;

Figure 8 shows a modification to the embodiment of Figures 1 and 2, in which a resilient strip is used to bias the die against the intermediate substrate;

Figure 9 shows a configuration of the invention in which a die receiving housing is used to retain a die face up;

Figure 10 shows a modification of the invention, in which an intermediate substrate is used to directly connect the die to an external connector connected to external test circuitry; and

Figure 11 shows a configuration in which an intermediate substrate extends over the die and a part of the die cavity plate which includes electrical contacts.

Detailed Description of the Preferred Embodiment

Referring to Figures 1 and 2, the inventive burn-in fixture 11 includes a die cavity plate, 13 and a cover 15. The die cavity plate 13 includes a die receiving cavity 17.

The die receiving cavity 17 has dimensions which are at least sufficient to accommodate a die 21. The die 21 is to be connected at bondpads 27, which are typically 0.1 mm wide. The die cavity plate 13 has a slot 31 which permits convenient access to the bottom of the die 21 in order that the die 21 may be lifted out of the die receiving cavity 17. Alignment of the die 21 in the die cavity plate 13 is achieved by aligning the cover 15 and die 21 to the bondpad 27.

A plurality of external connector leads 33 extend from the burn in fixture 11. As can be seen in Figure 2, in the preferred embodiment, the external connector leads 33 are attached to the die cavity plate 13, and extend therefrom.

The external connector leads 33 are shown as connector pins, which preferably are in a DIP (dual inline package) or QFP (quad flat pack) configuration.

The external connector leads 33 are secured by the die cavity plate 13 and terminate on the die cavity plate 13 with contact pads 37.

Referring to Figure 3, as well as Figures 1 and 2, an intermediate substrate 41 is used to extend between a wire connection to the contact pads 37 on the die cavity plate 13 and the bondpads 27. The intermediate substrate 41 includes a plurality of die contacts 43 which establish ohmic contact with the bondpads 27 or other test points on the die 21.

The intermediate substrate 41 is preferably formed of silicon, and includes a plurality of conductive circuit traces 45 thereon which communicate with substrate bondpads 47. The conductive traces 45 are preferably on a top surface 49 of the intermediate substrate 41. The substrate bondpads 47 are connected to the contact pads 37 by any convenient means, such as by wirebond. The use of silicon or other semiconductor material for forming the intermediate substrate 41 permits the contacts 43 and conductive traces 45 to be formed on the substrate by semiconductor circuit fabrication techniques, such as those used to form conductive lines and bondpads on semiconductors integrated circuit devices.

The intermediate substrate 41 may be formed as a rigid, semirigid, semiflexible or flexible material. In the case of silicon, as the substrate material, it is possible to form the

material thin enough that it is at least semiflexible. In the preferred embodiment, a rigid substrate is used.

In the preferred embodiment, the intermediate substrate 41 is substantially rigid. The rigidity is sufficient that, when the intermediate substrate 41 is aligned with the die 21, the height of the die contacts 43 nearly align in a Z axis direction with the bondpads 27 and that contact is established between the bondpads 27 and die contacts 43 without the need to significantly distort the intermediate substrate 41. Typically such contact is achieved at all desired points by allowing the die contacts 43 to be depressed, or by the use of a Z-axis anisotropic conductive interconnect material (67, Figure 7).

The intermediate substrate 41 may also be formed of other semiconductor process materials such as silicon on saphire (SOS), silicon on glass (SOG) or semiconductor process materials using semiconductor materials other than silicon.

The bondpads, as can be seen in Figure 4, are typically recessed below a top surface level 51, established by a BPSG passivation layer 53.

Alternatively, as shown in Figure 5, the intermediate substrate 41 may be formed from a ceramic material 55 onto which are formed a plurality of conductive traces 59. The conductive traces 59 have bumps 61 which are intended for registration with a bondpad 27, or a contact pad should the substrate 41 extend that far. The conductive traces 59 therefore are able to conduct signals between the bondpads 27

and the contact pads 37, provided that ohmic contact is established between the bondpads 27 and contact pads 37 and the respective bumps 61. It is also possible to use any other suitable interconnect, including for example flexible, rigid or semi-rigid polyimide tape.

In either the silicon or the ceramic substrate, the conductive traces and the die contacts 43 (Figure 3) or the bumps 61 (Figure 5), may be made of metal conductors or of any material which has significant conductivity, provided that the conductivity of the element is sufficient to permit electrical testing of the die.

The use of an intermediate substrate 41 allows dies with different patterns of bondpads 27 to be aligned with a version of the intermediate ~~circuit trace~~ substrate 41 custom made for that die, with several variants of the intermediate ~~circuit trace~~ substrate 41 mating with the same die cavity plate 13.

Since the intermediate substrate 41 also has the die contacts 43 thereon, the lifetime of the die contacts 43 is not directly determinative of the lifetime of the die cavity plate 13. Also, in the preferred embodiment, the external connector leads 33 are electrically connected to the contact pads 37 by internal conductors 65. The fact that the conductive traces 45 are on the top surface 49 of the intermediate substrate 41 facilitate the formation of elevated contacts on the die contacts 43, and allow the use of materials which are suitable for the formation of the elevated contacts.

The die 21 is placed on the intermediate substrate 41 with bondpads 27 on the die 21 aligned with the die contacts 43. Raised asperities 69 are located at the point of contact of the die contacts 43 with the bondpads 27. The raised asperities 69 are formed on the die contacts 43. In the case of a ceramic intermediate substrate, the asperities are formed by a combination of photoplating techniques and doinking. Other techniques for depositing material may be used in lieu of photoplating, such as stenciling, screen printing or direct writing. The doinking process is described in ~~copending U.S. Patent Application serial no. 7/898,617, filed 06/15/92, for PROCESS FOR FORMING RAISED SURFACE IRREGULARITIES BY ULTRASONIC FORGING, by Alan Wood, David Hembree and Warren Farnworth, and~~ U.S. Patent No. 5,249,450 Application serial no. 7/898,624 ~~(s.n. 7/898,625)~~, entitled ~~for~~ PROBEHEAD FOR ULTRASONIC FORGING, by Alan Wood, David Hembree, Larry Cromar and Warren Farnworth. It is anticipated that the intermediate substrate 41 may be repeatedly used, and the die contacts 43 re-doinked between uses.

As shown on Figure 6, the bumps 61 on the intermediate substrate 41 may be formed with raised portions 73. The raised portion 73 may penetrate the bondpad 27 or contact pad 37, while the remainder of the bump 61 functions to limit penetration depth of the raised portion 73. This permits the penetration depth of the bump 61 to be controlled by the physical dimensions of the raised portion 73. This results in the bumps 61 being self-limiting in their penetration of the bondpads 27, since the force required to cause the raised portion 73 to penetrate the bondpad 27 is significantly less than the force required for the remainder of the bump 61 to penetrate the bondpad 27.

The result is the raised portion 73 causes an indentation in the bondpad 27 but the indentation preferably is less than the thickness of the bondpad 27. The remainder of the bondpad beneath the bump 61 may be slightly distorted, but remains fully workable in subsequent assembly operations. for subsequent assembly operations, the bondpad 27 may be treated as if it were undamaged, and therefore the bondpad is considered not to be significantly damaged.

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The ratio of force will vary according to materials and dimensions, but ratios of at least 2:1 permissible force to required force are expected. If the percentage of the bump 61 which is raised 73 is sufficient, higher ratios, such as 4:1, 10:1 and greater may be expected. This is significant because variations in planarity may be expected on the intermediate substrate 41 and the die 21.

Figure 7 shows the use of a Z-axis anisotropic conductive interconnect material 77. The Z-axis anisotropic conductive interconnect material 77 functions as an interface between the intermediate substrate 41 and the bondpads or testpoints 27.

The Z-axis anisotropic conductive interconnect material 77 is particularly useful in cases in which the bondpads 27 are recessed below a BPSG passivation layer on the die 21. Other advantages of the Z-axis anisotropic conductive interconnect material 77 result from it being easily replaced when sequentially testing different dies 21 in the same package. The Z-axis anisotropic conductive interconnect material 77 is able to elastically deform in establishing

ohmic contact with the bondpads 27, so that replacement or redoinking of the intermediate substrate 41 may be required less often.

By using the raised asperities 69 of Figure ~~6~~ 7 or the bumps 61 of Figure 6, the pressure applied against the die 21 and the bondpad 27 by the Z-axis anisotropic conductive interconnect material 77 may be controlled. It is anticipated that the Z-axis anisotropic conductive interconnect material 77 may be caused to selectively penetrate the bondpad 27 so that the Z-axis anisotropic conductive interconnect material 77 will cause an indentation in the bondpad 27 which is less than the thickness of the bondpad 27. It is also anticipated that the remainder of the bondpad may be slightly distorted, but remains fully workable in subsequent assembly operations. The area of the bondpad 27 where force is applied to establish ohmic contact by the Z-axis anisotropic conductive interconnect material 77 is thereby controlled by the raised asperities 69 or by the topography of the bumps 61.

As can be seen in Figure 7, the bondpads 27 are in some cases recessed beneath the top surface of the die, as a result of the application of the passivation layer 53. The bondpads 27 also tend to be fragile. If the Z-axis anisotropic conductive interconnect material 77 is used to provide an interface between the bondpad 27 and the intermediate substrate 41, ohmic contact to be made through the Z-axis anisotropic conductive interconnect material 77, rather than directly between the intermediate substrate 41 and the bondpads 27. Conveniently, the Z-axis anisotropic conductive interconnect material is also able to extend between the

intermediate substrate 41 and the contact pads 37, thereby also facilitating the connection of the intermediate substrate 41 to the contact pads 37.

The use of the Z-axis anisotropic conductive interconnect material 77 between the bondpads 27 and the intermediate substrate 41 performs several functions. The ability of the Z-axis anisotropic conductive interconnect material to resiliently deform permits it to distort sufficiently to reach into the recesses defined by the bondpads 27. The compliant nature of the Z-axis anisotropic conductive interconnect material 77 permits ohmic contact to be made with the bondpads 27 with a minimum of damage to the bondpads. This is important in the burn in and testing of unpackaged die because it is desired that the bondpads remain substantially undamaged subsequent to burn in and testing. The compliant nature of the Z-axis anisotropic conductive interconnect material 77 permits an intermediate contact member such as the intermediate substrate 41 to be slightly misaligned with the bondpads 27. As long as there is a sufficient amount of material in the conductive path beneath the intermediate substrate 41 which is also in contact with the bondpads 27, ohmic contact will be established. It is also necessary to provide a biasing force to maintain ohmic contact. While the biasing force may be achieved by using a further elastomeric pad (79, shown in Figure 9), the elastomeric nature of the Z-axis anisotropic conductive interconnect material 77 is also able to provide some biasing force.

Significantly, the Z-axis anisotropic conductive interconnect material 77 need not be permanently bonded to the bondpads 27. Ohmic contact is established by biasing force. This enables the Z-axis anisotropic conductive interconnect material 77 and intermediate substrate 41 to be lifted from the die 21 without destroying the bondpads 27.

The Z-axis anisotropic conductive interconnect material 77 and intermediate substrate 41 therefore are able to conduct signals between the bondpads 27 and the die contacts 43.

It is also possible to permanently bond the Z-axis anisotropic conductive interconnect material 77 and the intermediate substrate 41 to the die 21, and to retain the attachment to the intermediate substrate 41 to the die 21 subsequent to burn in.

The cover 15 includes a rigid cover plate 81 and an optional resilient compressible elastomeric strip 83, which serves as a resilient biasing member, as shown in Figure 8. When the cover plate 81 is secured to the die cavity plate 13, the elastomeric strip 83 biases the Z-axis anisotropic conductive interconnect material 77 and intermediate substrate 41 against the die 21. This establishes an ohmic contact between the bondpads 27 and the conductive traces on the intermediate substrate 41, without the intermediate substrate 41 being bonded to the bondpads 27.

It has been found that an optimum technique for temporarily securing the intermediate substrate 41 in place in the die cavity plate 13 is the use of a precured RTV silicone

strip, commonly known as "gel pack," as a backing strip 85. The backing strip 85 exhibits a static charge sufficient and coefficient of friction sufficient to hold the intermediate substrate 41 in place without adhesive, and also is elastomeric. In other words, the silicone holds the silicon in place and biases the silicon against the intermediate substrate 41 and cover plate 81.

The elastomeric strip 83 is considered optional because it has been found that an optimum technique for temporarily securing the intermediate substrate 41 in place in the die cavity plate 13 is the use of the precured RTV silicone strip as a backing strip 85. With the use of the backing strip 85, the die 21 therefore is biased against the intermediate substrate 41 even without the use of the elastomeric strip 83, provided that the distances are appropriately selected to effect biasing.

The non-bonded contact of the Z-axis anisotropic conductive interconnect material 77 is significant at the bondpads 27. Contact between the intermediate substrate 41 and the contact pads 37 on the fixture 11 may be effected by bonding techniques. Such bonding is not expected to deteriorate the fixture 11, even though the fixture is used multiple times. If bonding is used for such contact, then the conductive material from the intermediate substrate may remain with the fixture 11, but without detriment to the operation of the fixture 11.

"Flip chip" optical alignment is used to align the cover plate 81 with the die cavity plate 13. A clamp 89 then secures the cover plate 81 in place over the die cavity plate 13. The clamp 89 may consist of a wire clasp which may either be latched into place against itself, as shown, or is fitted into parallel horizontal locations in the die cavity plate 13 and the cover plate 81. With the cover plate 81 in place, conductors on the intermediate substrate 41 extend from the bondpads 27 to the location of contact pads 37, so that the bondpads 27 are in electrical communication with the external connector leads 33.

In the preferred embodiment, the clamp 89 is part of an external clamping system as described in U.S. Patent No. ~~Serial No. 8/46,675, filed May 14, 1993~~ 5,367,253, entitled "CLAMPED CARRIER FOR TESTING OF SEMICONDUCTOR DIES". This patent ~~application~~ is hereby incorporated by reference.

Providing the intermediate substrate 41 allows the die 21 ~~is~~ to be placed face down, so as to establish connection between the bondpads 27 and die contacts 43. The Z-axis anisotropic conductive interconnect material 77 in this case is beneath the die 21. A precured RTV silicone backing strip ~~95~~ is used to secure the die 21 to ~~a~~ the cover plate ~~97~~ 81 and to bias the die 21 against the die contacts 43.

In an alternate embodiment of a package 101, shown in Figure 9, a die receiving housing 103 is used to retain a die 21 face up and an intermediate substrate 105 is placed above the die 21. The intermediate substrate 105 connects the die 21 to external test circuitry through connections on the die

cavity housing. The die receiving housing 103 contains a die receiving cavity 109, which supports the die 21 in alignment with electrical contacts 111 which align with bondpads 27 on the die 21.

If Z-axis anisotropic conductive interconnect material 77 is used, the Z-axis anisotropic conductive interconnect material 77 is positioned between the die 21 and the upper portion 105, so that the electrical connection is established between the bondpads 27 and the contacts 111, and hence with the connector pins 107.

Figure 10 shows a configuration in which a housing fixture 141 merely retains the die 21 in electrical communication with an intermediate substrate 143. The intermediate substrate 143 extends beyond the confines of the fixture 141 and terminates in an external connector 155. The Z-axis anisotropic conductive interconnect material 77, if used, is positioned between the intermediate substrate 143 and the die 21, so as to establish contact with the diepads 27.

Figure 11 shows a configuration in which an intermediate substrate 163 having conductors 165 is placed over a die 21. The die 21 is placed face up and bumps 167 on the substrate 163 face down to engage the bondpads 27. Advantageously, the substrate 163 may extend over the contact pads 37 on the die cavity plate 13. A second set of bumps 168 on the substrate 163 establish ohmic contact with the contact pads, which electrically connects the conductors 165 on the substrate 163 to the contact pads 37.

While specific locations for bondpads had not been specified, it is possible to test a variety of configurations, including the conventional arrangement of bondpads at the ends of the die 21. The invention may also be used for testing die configured for LOC (leads over chip), as well as other designs. In each of the above examples, the assembled fixture is adapted for testing with conventional test equipment, such as a burn-in oven. What has been described is a very specific configuration of a test fixture. Clearly, modification to the existing apparatus can be made within the scope of the invention. While the configuration of a standard DIP package has been shown in the drawings, it is anticipated that other package configurations may be used. Other common configurations include PGA (pin grid array), LCC (leadless chip carrier) and MCR (molded carrier ring) packages, as well as other package types. It is also likely that specialized package types will be used, in which the configuration relates to convenient burnin and test handling. Accordingly, the invention should be read only as limited by the claims.